Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.149”**

**.115”**

**.060”**

**SOURCE**

**GATE**

**Top Material: Al**

**Backside Material: CrNiAg**

**Gate = .020” X .025”**

**Source = .060” (see above)**

**Backside Potential: DRAIN**

**Mask Ref: HEX 2.7 55V GEN 5**

**APPROVED BY: DK DIE SIZE .115” X .149” DATE: 7/11/22**

**MFG: INT’L RECTIFIER THICKNESS .013” P/N: IRFC046N**

**DG 10.1.2**

#### Rev B, 7/1